

## **REMARKS**

### **Summary of the Office Action**

In the Office Action, claims 47-49, 51 and 53-55 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,034,800 to Marchisi (Marchisi). Applicants are appreciative of the indication that claims 50 and 52 would be allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims.

### **Summary of the Examiner's Interview**

Applicants are appreciative of the courtesies extended to Applicants' representative by Examiners Norris and Talbot during the personal Examiner's Interview conducted February 27, 2003. During the Examiner's Interview, the Examiners acknowledged that Marchisi failed to show or suggest at least the feature of "a plurality of conductive leads inserted through the peripheral side wall and the inner wall" recited in independent claim 47.

### **Summary of the Response**

Applicants have rewritten claims 50 and 52 as suggested by the Examiner and respectfully request that claims 50 and 52 be indicated as allowable. Applicants have amended claim 47 to correct grammatical errors. Accordingly, Applicants do not consider these amendments to be narrowing amendments responsive to a rejection. Based on the amendments above and the remarks below, Applicants respectfully request withdrawal of the rejections of claims 47-55.

### **The Rejection Under 35 U.S.C. § 102(b) in View of Marchisi**

Applicants respectfully point out that claim 47 recites, among other things, "a plurality of conductive leads inserted through the peripheral side wall and the inner wall." Marchisi fails to teach or suggest this feature.

As discussed during the Examiner's Interview, Marchisi shows in Figs. 1-4 and describes in column 2, lines 37-43 that "coplanar metal fingers [3a, 3b] extend outside the shell 4 passing through a gap between the matching edges of the two halves 4a and 4b." In column 3, lines 21-33, Marchisi describes that the halves 4a, 4b include "two spaced (double) lateral walls, 7a and

7a', 7b and 7b', respectively" and that "the encapsulation resin occasionally may extrude through [the] gaps." Thus, the walls 7a and 7b are separated by a gap as are the walls 7a' and 7b' and the metal fingers pass through the gap between the walls 7a and 7b and between the walls 7a' and 7b'.

As such, Marchisi fails to teach or suggest at least the feature of a plurality of conductive leads inserted through the peripheral side wall and the inner wall, as recited in claim 47.

Accordingly, Applicants respectfully request withdrawal of the rejection based on Marchisi and an indication of allowability for claim 47.

Claims 48, 49, 51 and 53-55 depend from allowable claim 47 and recite further features of the invention. For at least these reasons, claims 48, 49, 51 and 53-55 are also in condition for allowance.

**CONCLUSION**

In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims. Applicant respectfully invites the Examiner to contact the undersigned at 202.739.5983 if there are any outstanding issues that can be resolved via a telephone conference.


**EXCEPT** for any issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0310. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Attached hereto is a marked up version of the changes made by this amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

Respectfully submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the claims:**

Claims 47-55 have been amended as follows:

47. (Amended) A semiconductor die carrier comprising:  
a housing for holding at least one semiconductor die and including:  
an end surface having a perimeter; ~~and~~  
a peripheral side wall connected to the end surface, extending about the perimeter  
of the end surface and including an outer peripheral surface and an inner peripheral  
surface; and  
an inner wall within the perimeter of the end surface and including an outer  
surface spaced from and opposing the inner peripheral surface of the peripheral side wall,  
and an inner surface facing the center of the housing; and  
a plurality of conductive leads inserted through the peripheral side wall and the inner  
wall.

48. The semiconductor die carrier according to claim 47, further comprising a cavity  
extending between the inner peripheral surface of the peripheral side wall and the outer surface  
of the inner wall.

49. The semiconductor die carrier according to claim 48, further comprising a filler in the  
cavity to seal an interior of said housing.

50. (Amended) ~~The semiconductor die carrier according to claim 49,~~ A semiconductor die  
carrier comprising:

a housing for holding at least one semiconductor die and including:  
an end surface having a perimeter;

a peripheral side wall connected to the end surface, extending about the perimeter of the end surface and including an outer peripheral surface and an inner peripheral surface; and

an inner wall within the perimeter of the end surface and including an outer surface spaced from and opposing the inner peripheral surface of the peripheral side wall, and an inner surface facing the center of the housing;

a plurality of conductive leads inserted through the peripheral side wall and the inner wall;

a cavity extending between the inner peripheral surface of the peripheral side wall and the outer surface of the inner wall; and

a filler in the cavity to seal an interior of said housing, wherein the filler comprises an adhesive.

51. The semiconductor die carrier according to claim 49, further comprising a semiconductor die received on the end surface; and  
the inner wall encircles the semiconductor die.

52. (Amended) ~~The semiconductor die carrier according to claim 51, wherein the housing further comprises~~ A semiconductor die carrier comprising:

a housing for holding at least one semiconductor die and including:

an end surface having a perimeter;

a peripheral side wall connected to the end surface, extending about the perimeter of the end surface and including an outer peripheral surface and an inner peripheral surface;

an inner wall within the perimeter of the end surface and including an outer surface spaced from and opposing the inner peripheral surface of the peripheral side wall, and an inner surface facing the center of the housing; and

a plurality of spaced-apart ledges extending from the inner surface of the inner wall;

a plurality of conductive leads inserted through the peripheral side wall and the inner wall;  
a cavity extending between the inner peripheral surface of the peripheral side wall and the outer surface of the inner wall;  
a filler in the cavity to seal an interior of said housing; and  
a semiconductor die received on the end surface and encircled by the inner wall.

53. The semiconductor die carrier according to claim 47, wherein the leads are arranged in multiple spaced apart rows.

54. The semiconductor die carrier according to claim 47, wherein the plurality of leads each comprise a substantially L-shape.

55. The semiconductor die carrier according to claim 47, wherein the peripheral side wall comprises a first material and the end surface comprises a second material different from the first material.